

REMARKS

At the time the current Official Action was mailed, the Examiner rejected claims 12-25. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Rejections under 35. U.S.C. § 102

The Examiner rejected claim 12 under 35 U.S.C. § 102(e) as being anticipated by Michejda et al. (U.S. Patent App. No. 2002/0190344, hereinafter "Michejda et al."). Applicants respectfully traverse this rejection.

Legal Precedent

Anticipation under section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under section 102, a single reference must teach each and every limitation of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Accordingly, the Applicants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter. The prior art reference also must show the *identical* invention "*in as complete detail as contained in the ... claim*" to support a *prima facie* case of anticipation. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989).

Claim 12 Features Omitted from Cited Reference

Claim 12 recites, *inter alia*, "a transistor comprising "a drain terminal comprising a doped polysilicon material *disposed within a first shallow cavity formed in an isolation oxide region*" and "a source terminal comprising a polysilicon material *disposed within a second shallow cavity formed in the isolation oxide region.*" Italics added. One exemplary embodiment of this structure is illustrated in Figs. 3-6, which are fully described by the accompanying text in the present application. Specifically, in accordance with one exemplary embodiment, isolation oxide

58 is disposed within trenches 52, as illustrated in Fig. 3. Subsequently, cavities 60 are formed in the isolation oxide 58. A conductive material 64, such as polysilicon, is disposed within the cavities 60, as illustrated in Fig. 5. Finally, the structures are etched to form the source terminal 36 and the drain terminal 38 disposed within the shallow cavities 64 formed in the isolation oxide 58.

In contrast, Michejda et al. discloses a semiconductor device 100 in which doped material 170 is deposited in trenches 140, 145 *formed in the semiconductor substrate*. Isolation structures 150 are formed inside the trenches 140, 145, and doped material 170 is deposited in the substrate trenches 140, 145 on top of the isolation structures 150. *See* paras. 0033-0034; *see also* Fig. 1A.

The Examiner stated:

Michejda et al. discloses on figure 1A a transistor comprising a drain terminal 178 comprising a doped polysilicon material (para [0034], lines 5-6 and para [0058]) disposed within a first shallow cavity formed in an isolation oxide region 150 (para [0033], line[] 4); a source terminal 178 comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region; a channel 130 (para [0033], line 3) formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (para [0042]) coupled to each of the drain terminal and the source terminal; and a gate 120 (para [0032], line 2) disposed over the channel and comprising one conductive layer disposed over a gate oxide layer 122 (para [0032], lines 4-5). Final Office Action, page 2.

The Examiner analogized the isolation structures 150 in Michejda et al. to the isolation oxide region in claim 12. However, the Examiner has failed to identify shallow cavities formed in the isolation structures 150 in Michejda et al. as further recited in claim 12.

As noted in the present application, the term “cavity” is often used interchangeably with the word “trench” in that they are similar structures. However, “cavity” is used in this case to distinguish from a trench. As used in the present application, the “trench” refers to a structure

formed in the substrate 50, while the "cavity" refers to structures formed in the isolation oxide 58 disposed within the trench. *See* Application, page 11, lines 16-20.

Michejda et al. in no way discloses cavities formed *in the isolation oxide regions as recited in claim 12*. In Michejda et al., doped material is disposed over the isolation structures *within the substrate trenches*. Para. 0034; *see also* Fig. 10. In sharp contrast, claim 12 requires that the doped polysilicon material be disposed *in shallow cavities in the isolation oxide region*. This distinction is an important and novel element of claim 12.

The Examiner has not identified any element of Michejda et al. which is analogous to cavities *in the isolation oxide region* as recited in claim 12. On the contrary, the isolation structures 150 disclosed in Michejda et al. appear to be mound-like structures with no features that could conceivably be construed as trenches or cavities. *See* Fig. 1A. Finally, as Michejda et al. does not disclose cavities formed in an isolation oxide region, this prior art cannot possibly disclose disposing a doped polysilicon material inside said cavities as further recited in claim 12.

Because the Michejda et al. reference does not disclose the recited features discussed above, it cannot possibly anticipate claim 12. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claim 12.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 17, 18 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. in view of Tsuchiaki (U.S. Patent No. 6,271,566, hereinafter "Tsuchiaki"). Further, the Examiner rejected claims 13-16 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. as applied to claim 12. Still further, the Examiner rejected claims 19-21 and 23-35 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. and Tsuchiaki as applied to claims 17 and 22. Applicants respectfully traverse these rejections.

Legal Precedent

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Claims 17 and 22 Features Omitted from Cited References

Claim 17 recites, *inter alia*, a memory device comprising a storage device and a transistor, wherein the transistor comprises a drain terminal “disposed within a first shallow cavity *formed in an isolation oxide region*,” and a source terminal, “disposed within a second shallow cavity *formed in the isolation oxide region*.” Claim 22 recites, *inter alia*, a system comprising a processor and a memory device, wherein the memory device comprises a transistor comprising a drain terminal “disposed within a first shallow cavity *formed in an isolation oxide region*,” and a source terminal, “disposed within a second shallow cavity *formed in the isolation oxide region*.”

Tsuchiaki discloses a semiconductor integrated circuit device. The Examiner stated that Tsuchiaki teaches “a storage device connected to a transistor” and “a memory device coupled to the processor and comprising a storage device.” Citations omitted. As discussed above in relation to claim 12, the Examiner has failed to disclose any element in Michejda et al. which could be construed as a cavity formed in an isolation oxide region. In addition, nothing disclosed in Tsuchiaki cures these deficiencies of the Michejda et al. reference.

Because the Examiner has not shown that the cited combination includes all of the claimed elements, Applicants respectfully request withdrawal of the Examiner’s rejection and allowance of claims 17 and 22. In addition, Applicants respectfully request withdrawal of the Examiner’s

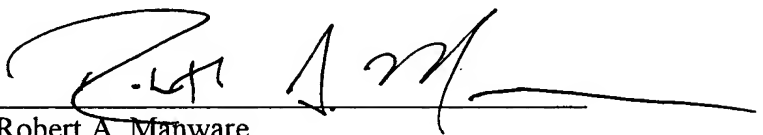
rejection and allowance of claims 13-16, 18-21 and 23-25 due to their dependence on allowable base claims.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of claims 12-25. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: August 5, 2005


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